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REMARKS

Applicants have amended claims 26-28 and 33-40 The specification has been amended to correct clerical errors in the title and in the written description. No new matter has been added.

The Examiner has objected to the drawings submitted as being informal. Formal drawings have been ordered and will be submitted in due course. It is requested that the requirements for formal drawings be deferred pending the allowance of the application. Applicant is unclear as to what the Examiner is referring in discussing "drawing corrections requested, but not made in the prior application," as there was no prior related application and no correction to the drawings has been requested. The formal drawings to be submitted will be renderings of the informal drawings filed with the application and will comply with the requirements of Form PTO 948 (Rev. 8-98).

Claims 26-32 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. patent number 5,313,101 (Harada et al.). Applicant respectfully traverses this rejection.

Claim 26, as amended, defines a semiconductor device having "a metalic layer over a substrate" and "an antireflective coating over said metallic layer" and also "a via hole extending through the dielectric layer and antireflective coating." This claim defines a device having a high integrity liner allowing for improvements in the elimination of void formation in a plug structure.

Harada et al. does not teach or suggest the device of claim 26. There is at least no teaching in Harada et al. of the antireflective coating over the metallic layer or of a via hole extending through a dielectric layer and an antireflective coating as claimed. Because Harada et al. does not teach or suggest every limitation of the semiconductor device as claimed, claim 26 is patentable over Harada et al.

Claim 27, as amended, defines a semiconductor device having "a dielectric layer on the aluminum layer" and "an antireflective coating over said dielectric layer" and "a via hole extending thorough the dielectric layer and said antireflective coating to a surface of the aluminum layer," and "a titanium aluminide layer lining at least a bottom of the via hole," and "a titanium nitride layer substantially free of through cracks formed on the titanium aluminide layer." This claim defines a device having a high integrity liner allowing for improvements in the elimination of void formation in a plug structure. For at least the same reasons set forth above for claim 26, claim 27 is patentable over Harada et al.

Claim 28, as amended, defines a semiconductor device including "a second dielectric layer on the first metallic layer," and "an antireflective coating over said second dielectric layer," and "a via hole extending through the second dielectric layer and the antireflective coating." This claim defines a device having a high integrity liner allowing for improvements in the elimination of void formation in a plug structure. Harada et al. does not teach or suggest the device of claim 28. For at least the same reasons set forth above for claim 26, claim 28 is patentable over Harada et al. Claims 29-32 depend from claim 28, and are therefore patentable over Harada et al. for at least the same reasons set forth for claim 28. Additionally, each depending claim, 29-32, is separately patentable because of its unique combination of limitations.

Because Harada et al. does not teach or suggest the claimed combination of limitations set forth in claims 26-32, each of these claims is patentable over Harada et al. Applicant respectfully requests that the 35 U.S.C. § 102 rejection of claims 26-32 be withdrawn.

Claims 33-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Harada et al. in view of U.S. patent number 4,656,605 (Clayton). Applicant respectfully traverses this rejection.

Claim 33, as amended, defines a memory module having chips having a semiconductor substrate including "a dielectric layer on the first metallic layer," and "an

antireflective coating over the dielectric layer," and "a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer." This claim defines a device having a high integrity liner allowing for improvements in the elimination of void formation in a plug structure, that device being incorporated into a greater apparatus structure. Neither Harada et al. alone, nor in combination with Clayton, teaches or suggests the device of claim 33. As discussed above regarding the 35 U.S.C. § 102 rejection of claim 26, Harada et al. at least does not describe a device having an antireflective coating or a via hole extending through an dielectric layer and an antireflective coating. Clayton can add no teaching or suggestion that can overcome this shortcoming of the description of Harada et al. Therefore, the subject matter of claim 33 would not have been obvious over Harada et al. in view of Clayton.

Claims 34-36, as amended, define memory modules incorporating memory chips having semiconductor substrates including similar limitations to those described above in relation to claim 33. Therefore, the subject matter of claims 34-36 would not have been obvious over Harada et al. in view of Clayton for at least the same reasons set forth above for claim 33.

Claims 33-36 are patentable over Harada et al. in view of Clayton. Therefore, Applicant respectfully requests that the 35 U.S.C. § 103 rejection of claims 33-36 be withdrawn.

Claims 37-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Harada et al. alone. Applicant respectfully traverses this rejection.

Claim 37, as amended, defines a computer system having a processor and a semiconductor chip including "a dielectric layer on the first metallic layer," and "an antireflective coating over said dielectric layer," and "a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer." For at least the same reasons set forth above regarding claims 26-36, Harada et al. does not teach or suggest the device of claim 37 and claim 37 is patentable over Harada et al.

Claims 38-40, as amended, define computer systems having a processor and a memory on a chip including similar limitations to those described above in relation to claim 37. Therefore, for at least the reasons set forth above for claim 37, the subject matter of claims 38-40 would not have been obvious over Harada et al.

Claims 37-40 are patentable over Harada et al. Therefore, Applicant respectfully requests that the 35 U.S.C. § 103 rejection of claims 37-40 be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Changes to the Specification:

FIG. 3 shows an enlarged view of a via fabricated according to a second embodiment of this invention. In this embodiment, the titanium aluminide 37 is formed in situ by heating a deposited titanium film 34 as a source material before further materials are deposited in the via hole 300. A titanium film 34 can be deposited by methods described earlier. After deposition of the titanium, the heating of the wafer can be conducted by transferring it in a vacuum to a heated pedestal where the titanium aluminide is formed, such as by using a CVD reactor-equipped cluster tool. Alternatively, the titanium film can be deposited in a single chamber using a heated pedestal to support the intermediate semiconductor workpiece such that titanium aluminide is formed rapidly as the elemental titanium is deposited on the exposed aluminum surface of aluminum conductor line 31. The dielectric layers [40] 30 and [43] 33 and the ARC layer [42] 32 are of the same types as described in connection with FIG. 1.

Changes to the Claims:

26. (Amended) A semiconductor device, comprising:
a metallic layer over a substrate;
an antireflective coating over said metallic layer;
a dielectric layer [on the metallic layer] over said antireflective coating;
a via hole extending through the dielectric layer and said antireflective coating to a surface of the metallic layer;
a titanium aluminide layer lining at least a bottom of the via hole; and
a conductive material formed on the titanium aluminide [liner] layer.

27. (Amended) A semiconductor device, comprising:

an aluminum layer over a substrate;

a dielectric layer on the aluminum layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and said antireflective coating to a surface of the aluminum layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

28. (Amended) A semiconductor memory device, comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over said second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.

33. (Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a first metallic layer over a substrate;

a dielectric layer on the first metallic layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

34. (Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a metallic layer over a substrate;

a dielectric layer on the metallic layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and said antireflective coating to a surface of the metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole; and

a conductive material formed on the titanium aluminide [liner] layer; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

35. (Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

an aluminum layer over a substrate;

a dielectric layer on the aluminum layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the aluminum layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

36. (Amended) A memory module, comprising:

a substrate comprising a circuit board;

a plurality of memory chips mounted on the substrate and connected to form a memory circuit, wherein one or more of the memory chips comprise a random access memory (RAM) fabricated on a semiconductor substrate comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over the second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material; and

an edge connector along one edge of the substrate which is wired to said memory circuit.

37. (Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a first metallic layer over a substrate;

a dielectric layer on the first metallic layer;

an antireflective coating over said dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the first metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material formed on the titanium compound layer; and

a second metallic layer on the dielectric layer and electrically connected to the plug material.

38. (Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a metallic layer over a substrate;

a dielectric layer on the metallic layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the metallic layer;

a titanium aluminide [layer lining] liner at least a bottom of the via hole; and

a conductive material formed on the titanium aluminide liner.

39. (Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

an aluminum layer over a substrate;

a dielectric layer on the aluminum layer;

an antireflective coating over the dielectric layer;

a via hole extending through the dielectric layer and the antireflective coating to a surface of the aluminum layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium nitride layer substantially free of through cracks formed on the titanium aluminide layer;

a conductive plug material on the titanium nitride layer; and

a metallic layer on the dielectric layer and electrically connected to the plug material.

40. (Amended) A computer system, comprising:

a processor; and

a random access memory (RAM) fabricated on a semiconductor chip communicating with the processor and comprising:

a memory circuit region in a semiconductor substrate;

a first dielectric layer over the memory circuit region;

a first metallic layer over the first dielectric layer;

a contact interconnect between the first metallic layer and the substrate;

a second dielectric layer on the first metallic layer;

an antireflective coating over the second dielectric layer;

a via hole extending through the second dielectric layer and the antireflective coating to a surface of the second metallic layer;

a titanium aluminide layer lining at least a bottom of the via hole;

a titanium compound layer formed on the titanium aluminide layer;

a conductive plug material on the titanium compound layer; and

a second metallic layer on the second dielectric layer and electrically connected to the plug material.

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Respectfully submitted,

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